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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,502	03/08/2004	David Mendel	174/308	3014

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EXAMINER	
BROWN, MICHAEL J	
ART UNIT	PAPER NUMBER
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,502	MENDEL ET AL.	
	Examiner	Art Unit	
	Michael J. Brown	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-95* is/are pending in the application.

4a) Of the above claim(s) *1-28,40-55,57-80,85-88 and 90-95* is/are withdrawn from consideration.

5)☒ Claim(s) *30,35 and 36* is/are allowed.

6)☒ Claim(s) *29,31-34,37-39,56,81-84 and 89* is/are rejected.

7)☒ Claim(s) *30,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/30/04 and 9/13/05*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20070207*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 9/30/04 and 9/13/05 was filed. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to because in Figure 18 Block 1860 should be 1850 and block 1870 should be 1860 according to the Specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If

the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Allowable Subject Matter

3. Claims 30, and 35-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 81-84 and 89 are rejected under 35 U.S.C. 102(b) as being anticipated by Hart et al.(US Patent 6,621,325).

As to claim 81, Hart discloses a programmable logic device(field programmable gate array(FPGA); see Fig. 3) comprising a plurality of transistors(logic sets in CLBs 00, 01, 02, 10, 11, 12, 20, 21, and 22; see Fig. 3), a first sub-plurality of said transistors being used for a design implemented in the programmable logic device(see column 8,

lines 1-2), and a second sub-plurality of said transistors not being used for said design(see column 8, lines 1-2), and means for reverse-biasing at least some of the transistors in the second sub-plurality in order to reduce leakage current(see column 7, lines 61-67).

As to claim 82, Hart discloses the device wherein the means for reverse-biasing is at least partly dynamically operable during programmable logic device operation(see column 7, lines 61-62).

As to claim 83, Hart discloses the device further comprising means for forward biasing at least some of said transistors that are not being reverse biased by the means for reverse biasing in order to speed up the operation of the transistors that are forward biased(see column 7, lines 37-39 and lines 60-61).

As to claim 84, Hart discloses the device wherein the means for forward biasing is at least partly operable during operation of the logic device(see column 7, lines 60-61).

As to claim 89, Hart discloses a method for increasing speed of signal propagation in a programmable logic device(field programmable gate array(FPGA); see Fig. 3), the programmable logic device comprising a plurality of transistors(logic sets in CLBs 00, 01, 02, 10, 11, 12, 20, 21, and 22; see Fig. 3), the method comprising evaluating whether a first transistor or group of transistors is used for a design implemented in the programmable logic device(see column 8, lines 1-2), if the first transistor or group of transistors is not used for the design, evaluating a second transistor or second group of transistors(see column 8, lines 1-2), if the first transistor or

group of transistors is used for the design, determining whether the first transistor or group of transistors can be forward biased to operate in a high speed mode(determined whether path is a "critical" or "non-critical" path, if "critical" then it can be forward biased; see column 6, lines 46-47 and column 7, lines 60-61), and if the first transistor or group of transistors can be forward biased to operate in a high speed mode and a programmable logic device power consumption specification and a programmable logic device routability specification permit, forward biasing the first transistor or group of transistors to operate in high speed mode(see column 7, lines 37-39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 29, 31-34, 37-39, and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hart et al.(US Patent 6,621,325) in view of Kang et al.(US Patent 6,759,873).

As to claim 29, Hart discloses a method for reducing power consumption in a programmable logic device(field programmable gate array(FPGA); see Fig. 3), the programmable logic device comprising a plurality of transistors(logic sets in CLBs 00, 01, 02, 10, 11, 12, 20, 21, and 22; see Fig. 3), the method comprising evaluating whether a first transistor or group of transistors is used for a design implemented in programmable logic device(see column 8, lines 1-2), if the first transistor or group of transistors is not used for the design, evaluating a second transistor or group of transistors(see column 8, lines 1-2), if the first transistor or group of transistors is used for the design, determining whether first transistor or group of transistors can be reverse biased to operate in a low power mode(determined whether path is a "critical" or "non-critical" path, if "non-critical" then it is the "slowest path" and can be reverse biased; see column 6, lines 46-47 and column 7, lines 61-62), and if the first transistor or group of can be reverse biased to operate in a low power mode and a programmable logic device speed specification and a programmable logic device routability specification permit, reverse biasing the first transistor or group of transistors to operate in low power mode(see column 7, lines 61-62). However, Hart fails to specifically disclose the reverse biasing occurring in a low power mode.

Kang teaches the reverse biasing occurring in a low power mode(standby mode; see column 3, line 40). It would have been obvious to one of ordinary skill in the art at

the time the invention was made to combine the inventions of Hart and Kang to establish reverse biasing transistors in a standby mode. The motivation to do so would be to consume less power especially when power is needed least.

As to claim 31, Hart discloses the method wherein the evaluating occurs during a routing period relating to the first transistor or group of transistors(see column 6, line 57- column 7, line 3).

As to claim 32, Hart discloses the method wherein the evaluating occurs following a routing period relating to the first transistor or group of transistors(see column 6, line 57- column 7, line 3).

As to claim 33, Hart discloses the method wherein the evaluating occurs during a placement period relating to the first transistor or group of transistors(see column 6, line 57- column 7, line 3).

As to claim 34, Hart discloses the method further comprising determining the change in speed of a function associated with the first transistor or group of transistors, the change in speed that is attributable to the reverse biasing(see column 7, lines 9-14).

As to claim 37, Hart discloses the method further comprising dynamically reverse biasing a plurality of transistors based on signals received via an input pin(see column 5, lines 32-40).

As to claim 38, Hart discloses the method further comprising utilizing at least one of synthesis programming, logic placement programming and routing programming to over-achieve timing goals in a portion of the programmable logic device in order to allow

at least one transistor to be reverse biased while still meeting performance requirements for the programmable logic device(see column 7, lines 1-14).

As to claim 39, Hart discloses the method further comprising grouping a plurality of signal routes into a region of the programmable logic device, the plurality of signal routes comprising transistors that may be reverse biased while maintaining the programmable logic device speed specification and the programmable logic device routability specification(see column 7, lines 1-14).

As to claim 56, Hart discloses a method for reducing power consumption in a programmable logic device(field programmable gate array(FPGA); see Fig. 3), the programmable logic device comprising a plurality of transistors(logic sets in CLBs 00, 01, 02, 10, 11, 12, 20, 21, and 22; see Fig. 3), the method comprising evaluating whether a first transistor is used for a design implemented in the programmable logic device(see column 8, lines 1-2), if the first transistor is not used for design, evaluating a second transistor(see column 8, lines 1-2), if the first transistor is used for the design, determining whether the first transistor can be reverse biased to operate in a low power mode(determined whether path is a "critical" or "non-critical" path, if "non-critical" then it is the "slowest path" and can be reverse biased; see column 6, lines 46-47 and column 7, lines 61-62), and if the first transistor can be reverse biased to operate in a low power mode and a programmable logic device speed specification a programmable logic device routability specification permit, reverse biasing first transistor to operate in low power mode(see column 7, lines 61-62). However, Hart fails to specifically disclose the reverse biasing occurring in a low power mode.

Kang teaches the reverse biasing occurring in a low power mode(standby mode; see column 3, line 40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the inventions of Hart and Kang to establish reverse biasing transistors in a standby mode. The motivation to do so would be to consume less power especially when power is needed least.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Brown whose telephone number is (571)272-5932. The examiner can normally be reached Monday-Thursday from 7:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571)272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael J. Brown
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REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
2/20/07